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Jie Zhang,[1,2] Adam Charnas,[1,2] Zehao Lin,[1,2] Dongqi Zheng,[1,2] Zhuocheng Zhang,[1,2] Pai-Ying Liao,[1,2] Dmitry Zemlyanov,[2] and Peide D. Ye[1,2,a)]

AFFILIATIONS

[1]Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA
[2]Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA

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[a)]**Author to whom correspondence should be addressed:** yep@purdue.edu

ABSTRACT

In this Letter, we report the electrical performance improvement of indium oxide (In_2O_3) thin film transistors (TFTs) via a low-temperature CF_4/N_2O plasma treatment. It is found that the fluorination via CF_4/N_2O plasma can reduce the excessive electrons in the In_2O_3 channel more effectively compared to the oxidative annealing, providing the same low off-currents at a lower temperature of 200 °C, while the hydrogenation could not give rise to the off-current reduction. The fluorinated In_2O_3 TFTs with a channel thickness of 3.5 nm, a HfO_2 dielectric thickness of 3.5 nm, and a channel length ranging from 80 nm to 1 μm demonstrate markedly improved electrical performances, including a high field effect mobility of 72.8 cm^2/V s, a more positive threshold voltage, a higher on/off current ratio of $\sim 10^6$, a smaller subthreshold swing below 200 mV/dec, and a higher stability to both negative and positive gate biases. X-ray photoelectron spectroscopy (XPS) confirms the fluorine incorporation in In_2O_3/HfO_2 heterojunction upon CF_4/N_2O plasma, speculatively passivating the oxygen vacancies and explaining TFT performance enhancement. This study suggests that the anion doping such as fluorine incorporation could be an effective method to improve the performance of oxide semiconductor TFTs with ultrathin channel and dielectric.

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Recent work on atomically thin atomic-layer-deposited (ALD) indium oxide (In_2O_3) thin film transistors (TFTs) has revitalized the prospects of In_2O_3 as a TFT channel material.[1–7] High performance In_2O_3 TFTs with a channel length (L_{ch}) of 8 nm and a channel thickness (T_{ch}) of 2.5 nm exhibit a record high on-current (I_{on}) of 3.1 A/mm and a record high transconductance (g_m) of 1.5 S/mm,[1] which is the best among all the known semiconductor thin film in the thickness range of 1.0–3.5 nm. The full device fabrication process incurs a thermal budget of just 225 °C, qualifying In_2O_3 as a strong candidate for back-end-of-line (BEOL) 3D integration applications. Furthermore, benefiting from the excellent conformity and large-area uniformity enabled by ALD growth, In_2O_3 TFTs on arbitrary large wafers and with complex 3D structures such as fin structures[3] and vertical multilayer stacks[2] can be fabricated. Historically, the main challenge for achieving high-performance In_2O_3 TFTs lays in that the bulk material shows almost metallic behavior with degenerate carrier concentration, making TFTs hard to deplete by conventional dielectric gating.[6] This issue can be resolved by three methods in previous reports: (1) channel thickness reduction: the bandgap of In_2O_3 is increased with the reduced T_{ch} due to quantum confinement, thus trap neutral level (TNL) can be modulated into bandgap, reducing excessive electrons;[6] (2) oxidative treatment: the In_2O_3 channel is treated in oxidative environment, such as high-temperature O_2 annealing[1,7] or O_2 plasma,[5] reducing oxygen vacancy-induced electrons; (3) metal cation doping: the In_2O_3 channel is doped with proper amount of other metal cation as carrier suppressor and strong oxygen binder, such as Ga,[8,9] Zn,[8,9] Sn,[10,11] W,[12] etc.

In this work, we report the performance improvement of In_2O_3 TFTs via low-temperature CF_4/N_2O plasma treatment at 200 °C in addition to the second approach described above. Although fluorine incorporation has been reported as an effective method of improving oxide TFT performance in a number of papers,[13–19] these works are all focused on oxide TFTs with large device dimension and thick channel/dielectric stack (Table S1, supplementary material), where

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fluorine mainly passivates the defects in the oxide channel. However, in the scaled oxide TFTs aimed at BEOL-compatible monolithic 3D integration, surface chemistry may play a more important role due to the nature of ultrathin oxide channel. Thus, it is highly demanded to investigate whether fluorine incorporation could still be effective for oxide TFT with the scaled device dimension. In this work, fluorinated In_2O_3 TFTs with a 3.5 nm thick HfO_2 dielectric, T_{ch} of 3.5 nm, and L_{ch} down to 80 nm are demonstrated, showing excellent electrical performance including a high μ_{FE} of 72.8 $cm^2/V\,s$, a more positive V_T, a higher I_{on}/I_{off} of $\sim 10^6$, subthreshold swing (SS) below 200 mV/dec, and a high stability to both negative and positive gate bias stress, which can be compared favorably with other recently reported oxide TFTs (Table S2, supplementary material). The surface chemistry between In_2O_3 channel and HfO_2 dielectric upon fluorination and oxidation is also elucidated by x-ray photoelectron spectroscopy (XPS). This study suggests that the fluorine incorporation could also be applied in oxide TFTs with scaled device dimensions for monolithic 3D integration.

Figure 1(a) shows a schematic illustration of back-gated long-channel In_2O_3 TFT for investigating various surface treatments, where p^+ Si ($\sim$0.005 Ω cm) and 90 nm thermally grown SiO_2 nm are used as the gate stack. The fabrication process started with the deposition of 3.5 nm In_2O_3 on cleaned Si/SiO_2 substrates by ALD at 225 °C with $(CH_3)_3In$ (TMIn) and H_2O as the In and O precursors, respectively. Then, In_2O_3 mesas were formed by BCl_3/Ar dry etching. Finally, 40 nm Ni was deposited by e-beam evaporation to form the source/drain contacts, defined by photolithography. The fabricated TFTs have a channel width (W_{ch}) of 70 μm and a L_{ch} of 6–20 μm. After initial DC electrical measurement, these long-channel In_2O_3 TFTs were subjected to O_2 annealing at 200, 250, and 300 °C, forming gas (FG) annealing (96% N_2 and 4% H_2) at 250 °C, and CF_4/N_2O plasma at 200 °C (named "CF_4-treated" hereafter). All of the treatments were done for 1 min. The CF_4/N_2O plasma treatment was conducted in a PECVD chamber, with an RF power of 200 W and the CF_4 and N_2O gas flow of 20 and 200 sccm, respectively. The CF_4 functions as the fluorine source, while the addition of N_2O could remove carbon, possibly increase the incorporated fluorine concentration by diluting CF_x radicals, and suppress the oxygen vacancies by providing an oxidative environment.[14,20] The O_2 and FG annealing was performed in a rapid thermal annealing (RTA) tool, with a gas flow of 2000 sccm. These long-channel In_2O_3 TFTs were adopted due to the high thermal stability of SiO_2 and the simplicity of the fabrication process.

Figure 1(b) shows transfer curves of representative In_2O_3 TFTs with a L_{ch} of 6 μm under drain-to-source voltage (V_{DS}) of 1 V after various surface treatments. The as-deposited and FG-annealed In_2O_3 TFTs show almost no gate modulation, suggesting that In_2O_3 channel is degenerate and cannot be depleted by the SiO_2/Si gate stack. This

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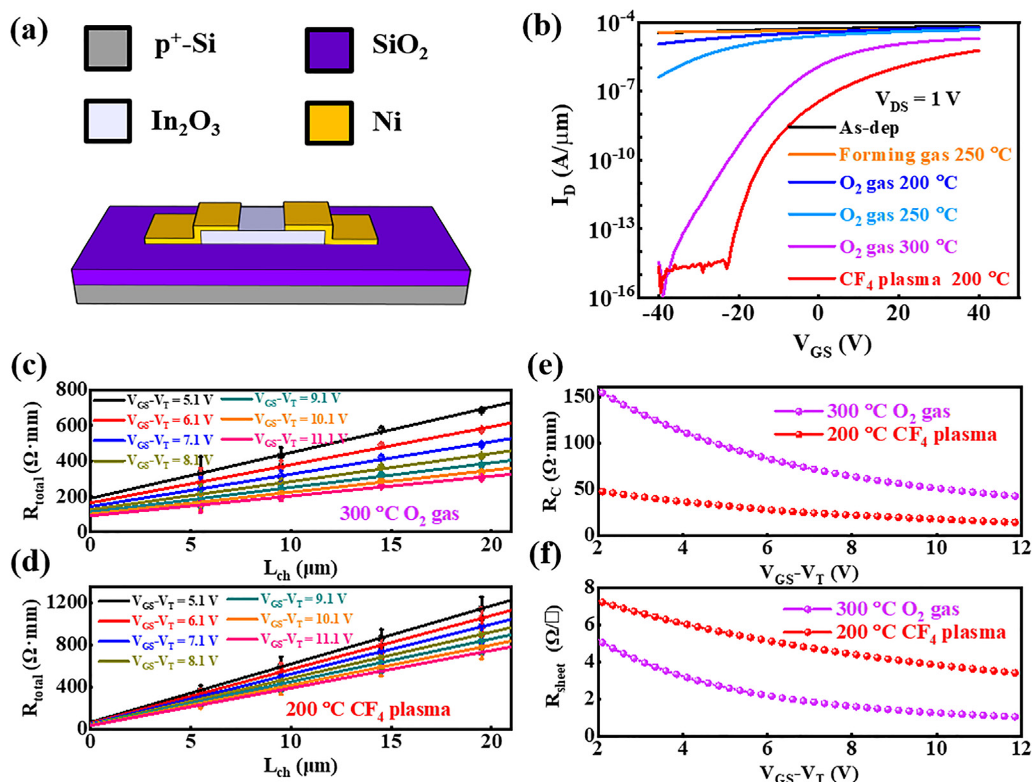

FIG. 1. (a) Schematic of long-channel In_2O_3 TFTs for investigating various surface treatments. (b) Transfer characteristics of In_2O_3 TFTs upon various treatment with a W_{ch} of 70 μm and a L_{ch} of 6 μm under V_{DS} of 1 V. Transfer length method measurements of In_2O_3 TFTs after (c) O_2 annealing at 300 °C, and (d) CF_4/N_2O plasma at 200 °C. Error bars represent one standard deviation from the average of five TFTs. (e) Extracted R_C and (f) R_{sheet} of O_2-annealed and CF_4-treated In_2O_3 TFTs as functions of the gate overdrive voltage.

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also indicates that hydrogenation might not resolve the degenerate carrier concentration issue in In_2O_3, which can be explained by the fact that H typically functions as a shallow donor in oxides.[9] On the other hand, upon O_2 annealing and CF_4/N_2O plasma, In_2O_3 TFTs start to exhibit greatly improved gate modulation with a reduced I_{off}. After CF_4/N_2O plasma at 200 °C, In_2O_3 TFTs show a low I_{off} of $\sim 10^{-15}$ A/μm (the detection limitation of our measurement), whereas the same low I_{off} can only be observed for TFTs after 300 °C O_2 annealing, suggesting that fluorination via CF_4/N_2O plasma is more effective in reducing the excess electrons in In_2O_3 channel compared to the oxidative annealing. Transfer length method (TLM) measurements were performed on 300 °C O_2-annealed [Fig. 1(c)] and 200 °C CF_4-treated [Fig. 1(d)] In_2O_3 TFTs, where at least five TFTs with the same L_{ch} were measured. The extracted contact resistance (R_C) and sheet resistance (R_{sheet}) as functions of V_{GS}–V_T are plotted in Figs. 1(e) and 1(f), respectively. The CF_4-treated In_2O_3 TFTs exhibit a smaller R_C and a larger R_{sheet} compared to that of O_2-annealed TFTs, which can be explained by the greater effectiveness of fluorination in reducing the excess electrons in the In_2O_3 channel and the low temperature of CF_4/N_2O plasma causing less degradation to the Ni contacts, benefiting the performance of scaled TFTs potentially. The degradation of Ni/In_2O_3 contact after high-temperature annealing could be due to the diffusion of Ni into In_2O_3, forming a NiO_x interfacial layer as a transport barrier.

The beneficial effects of fluorination were further verified by measurements on scaled short-channel In_2O_3 TFTs with 3.5 nm HfO_2 as the gate dielectric, the schematic of which is shown in Fig. 2(a). The fabrication process is described in detail in previous work.[1] Briefly, a 10 nm Al_2O_3 was first deposited by ALD at 175 °C to obtain a smooth surface on the Si/SiO_2 substrates. Then, 40 nm Ni bottom gates were deposited by e-beam evaporation, defined by a bilayer photolithography process. Next, 3.5 nm HfO_2 was deposited by ALD at 200 °C, followed by the deposition of 3.5 nm In_2O_3 by ALD at 225 °C. Then, In_2O_3 mesas were formed by BCl_3/Ar dry etching. Finally, 40 nm Ni was deposited as source/drain contacts by e-beam evaporation, defined by electron beam lithography. The fabricated In_2O_3 TFTs have a W_{ch} of 2 μm and a L_{ch} ranging from 1 μm to 80 nm. After initial electrical measurement, these short-channel In_2O_3 TFTs underwent O_2 annealing at 300 °C and CF_4/N_2O plasma at 200 °C for 1 min.

Figures 2(b)–2(d), respectively, illustrate the transfer curves and gate leakage currents (I_G) of the as-deposited, O_2-annealed, and CF_4-treated In_2O_3 TFTs with various L_{ch} under V_{DS} of 50 mV. The as-deposited In_2O_3 TFTs show good gate modulation, in contrast to no modulation in the long-channel In_2O_3 TFTs using SiO_2 as dielectric, due to the much stronger electrostatic control from the ultrathin high-κ HfO_2 dielectric and a better interface between the HfO_2 and In_2O_3. The I_{off} in all In_2O_3 TFTs is limited by the I_G from the ultrathin HfO_2 dielectric. A significantly increased I_G can be observed upon O_2

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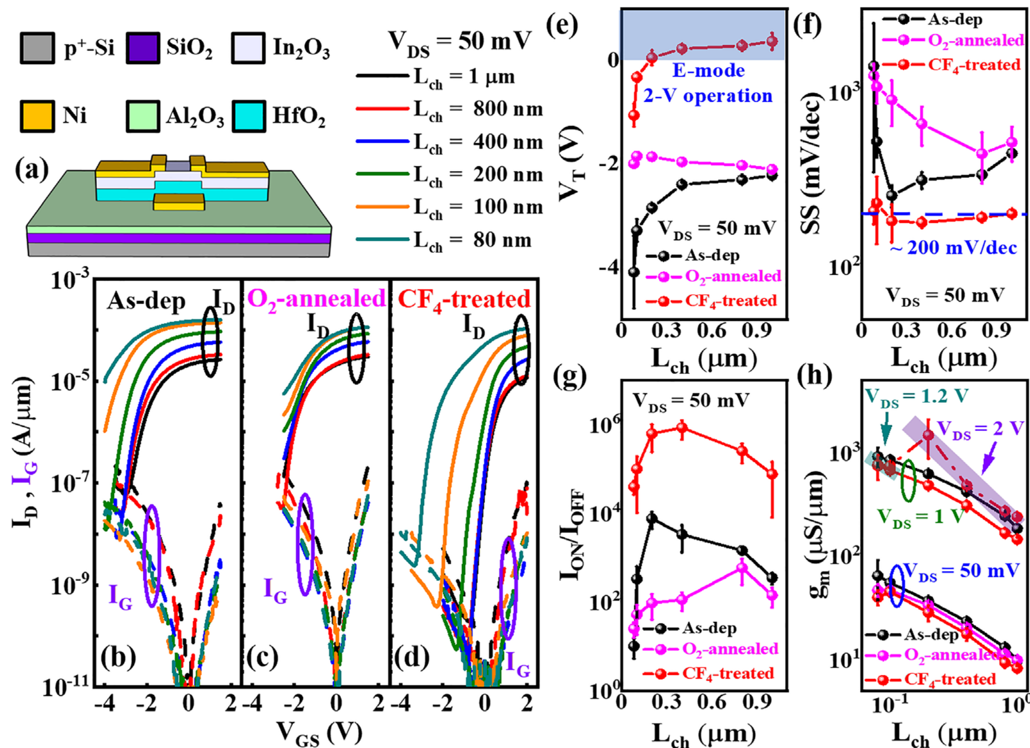

FIG. 2. (a) Schematic of a short-channel In_2O_3 TFT. Transfer characteristics and gate leakages of (b) the as-deposited, (c) O_2-annealed (300 °C), (d) CF_4-treated (200 °C) In_2O_3 TFTs with a W_{ch} of 2 μm and a L_{ch} ranging from 1 μm to 80 nm under V_{DS} of 50 mV. Statistical results of (e) V_T, (f) SS, (g) I_{ON}/I_{OFF}, and (h) g_m as functions of L_{ch} for the as-deposited, O_2-annealed, and CF_4-treated In_2O_3 TFTs. A higher V_{DS} can be applied in the CF_4-treated TFTs for g_m comparison. Error bars represent one standard deviation from the average of five TFTs.

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annealing, whereas a markedly reduced I_G is exhibited after CF_4/N_2O plasma. The increased I_G after O_2 annealing can be attributed to possible crystallization of HfO_2 at 300 °C temperatures.[21] The reduced I_G after CF_4/N_2O plasma suggests an improved dielectric quality of HfO_2, which agrees with previous reports that fluorine could passivate defects in HfO_2 and thereby reduce the leakage currents.[22,23] Figures 2(e)–2(g), respectively, illustrate the statistical results of V_T, SS, and I_{on}/I_{off} as a function of L_{ch} under V_{DS} of 50 mV with the different treatments. The CF_4-treated In_2O_3 TFTs show significantly improved performance including a more positive V_T, a smaller SS of ∼200 mV/dec, and a high I_{on}/I_{off} of $\sim 10^6$. Figure 2(h) compares the transconductance (g_m) of In_2O_3 TFTs after treatment, where both O_2-annealed and CF_4-treated In_2O_3 TFTs exhibit a slightly lower g_m compared to that of the as-deposited TFTs under V_{DS} of 50 mV, possibly due to a smaller mobility arising from a reduced carrier concentration. The CF_4-treated In_2O_3 TFTs exhibit a high μ_{FE} of $72.8 \pm 3.7\ cm^2/V\,s$ extracted from five TFTs with L_{ch} of 1 μm, which is only slightly smaller than that of the as-deposited TFTs with μ_{FE} of $86.4 \pm 9.8\ cm^2/V\,s$. The oxide capacitance C_{ox} of 2.27 $\mu F/cm^2$ is applied for mobility extraction. The reduced μ_{FE} with the decreased carrier concentration and enhancement-mode operation could be explained by the percolation conduction mechanism in oxide semiconductors.[8,9,12] Fortunately, the slightly reduced g_m and μ_{FE} could be compensated by the application of a higher V_{DS} in CF_4-treated In_2O_3 TFTs, benefiting from the better dielectric quality after CF_4/N_2O plasma. A high g_m of ∼1.48 S/mm can be achieved for CF_4-treated In_2O_3 TFTs with a L_{ch} of 200 nm, which is very close to that of 1.5 S/mm using ultra-scaled In_2O_3 TFTs with a L_{ch} of 8 nm in Ref. 1. Such a high V_{DS} cannot be applied to the as-deposited and O_2-annealed In_2O_3 TFTs, where severe self-heating and high I_G would cause TFT breakdown, thus demonstrating the superiority of CF_4/N_2O plasma treatment.

Figure 3 presents the transfer curves under various V_{DS} and the corresponding output characteristics of the representative CF_4-treated In_2O_3 TFTs with a L_{ch} of 80 nm, 200 nm, and 1 μm. The pinch-off and current saturation can be clearly observed in 200 nm and 1 μm TFTs and at low V_{GS} in 80 nm TFTs. It should be mentioned that the In_2O_3 TFTs with a L_{ch} beyond 200 nm are operational within 2 V, coupled with a low temperature process, showing a great promise for future portable and flexible electronics where battery-powered operation is required, in addition to BEOL-compatible logic and memory applications.[24] Gate bias stress instability tests were also performed on the as-deposited and CF_4-treated In_2O_3 TFTs with a L_{ch} of 80 nm, while the O_2-annealed TFTs were avoided due to the high I_G. The gate bias stress instability results under a positive gate stress bias ($V_{G,\,STR}$) of +2 V and a negative $V_{G,\,STR}$ of −4 V up to 2000 s at room temperature can be found in Fig. 4, with the source and drain being grounded during gate stress. The CF_4-treated In_2O_3 TFTs exhibit a much high stability to the gate bias, with a maximum V_T shift of −0.03 and +0.15 V for positive bias instability (PBI) and negative bias instability (NBI) tests, respectively, in contrast to the relatively large V_T shifts of −0.54 (PBI) and +0.56 V (NBI) observed in the as-deposited In_2O_3 TFTs. As a result, CF_4/N_2O plasma can also improve the gate bias stability of In_2O_3 TFTs significantly, which is of great importance for practical applications.

X-ray photoelectron spectroscopy (XPS) was performed on In_2O_3/HfO_2 heterojunction to unveil the interface chemistry. Figure 5(a) shows the survey spectrum, where fluorine can only be found in CF_4-treated

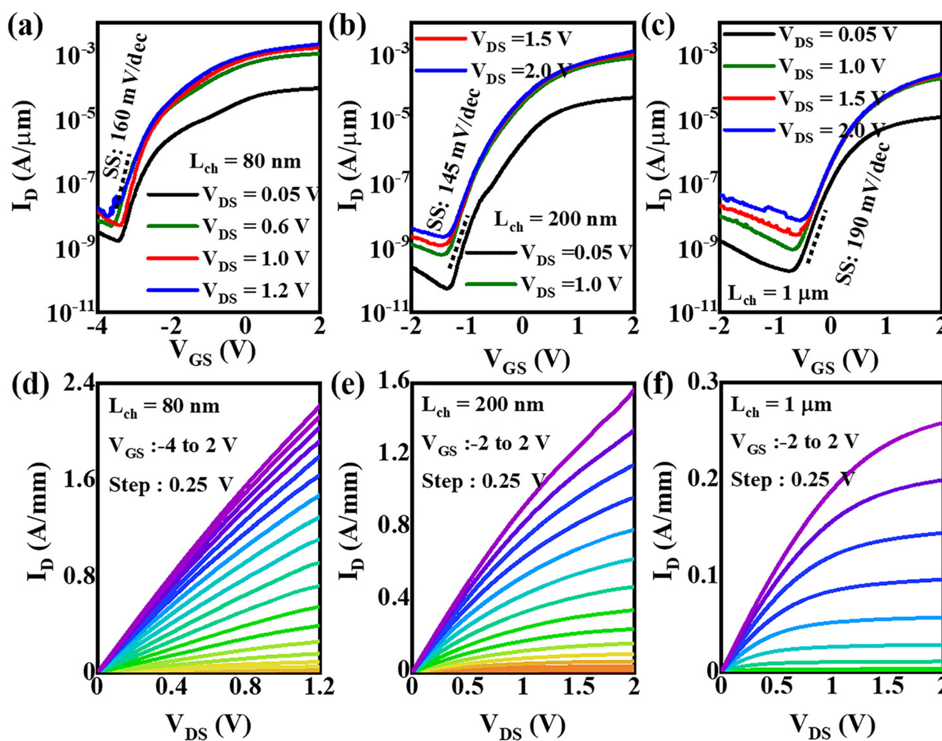

FIG. 3. Transfer curves at various V_{DS} of representative CF_4-treated In_2O_3 TFTs with a L_{ch} of (a) 80 nm, (b) 200 nm, and (c) 1 μm. The corresponding output characteristics of In_2O_3 TFTs with a L_{ch} of (d) 80 nm, (e) 200 nm, and (f) 1 μm.

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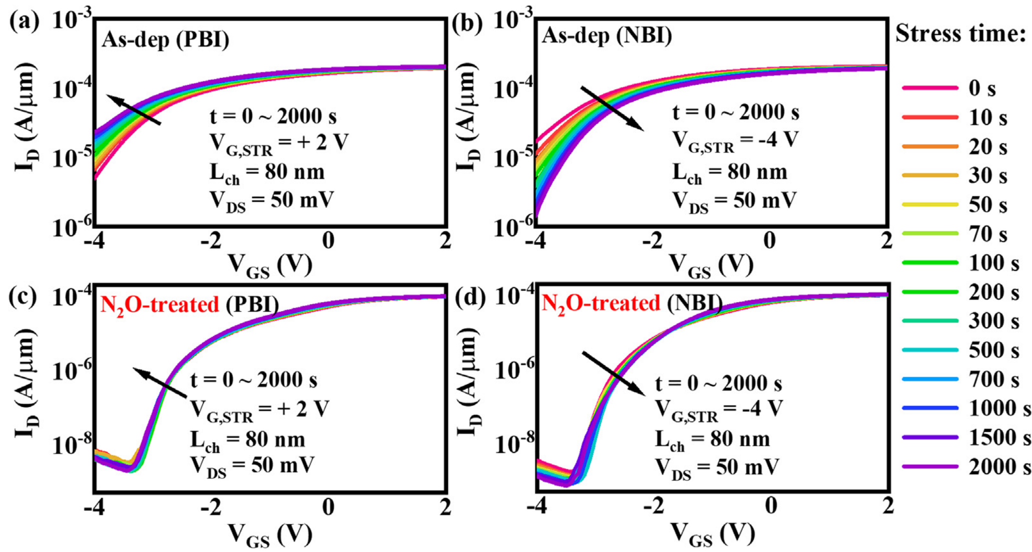

FIG. 4. Gate bias instability results of the as-deposited In_2O_3 TFTs with a L_{ch} of 80 nm for (a) positive gate bias instability (PBI) test and (b) negative gate bias instability (NBI) test. The corresponding gate bias instability results of the CF_4-treated In_2O_3 TFTs for (c) PBI and (b) NBI test. The significant improvement of both NBI and PBI using the same process is a very special and important observation.

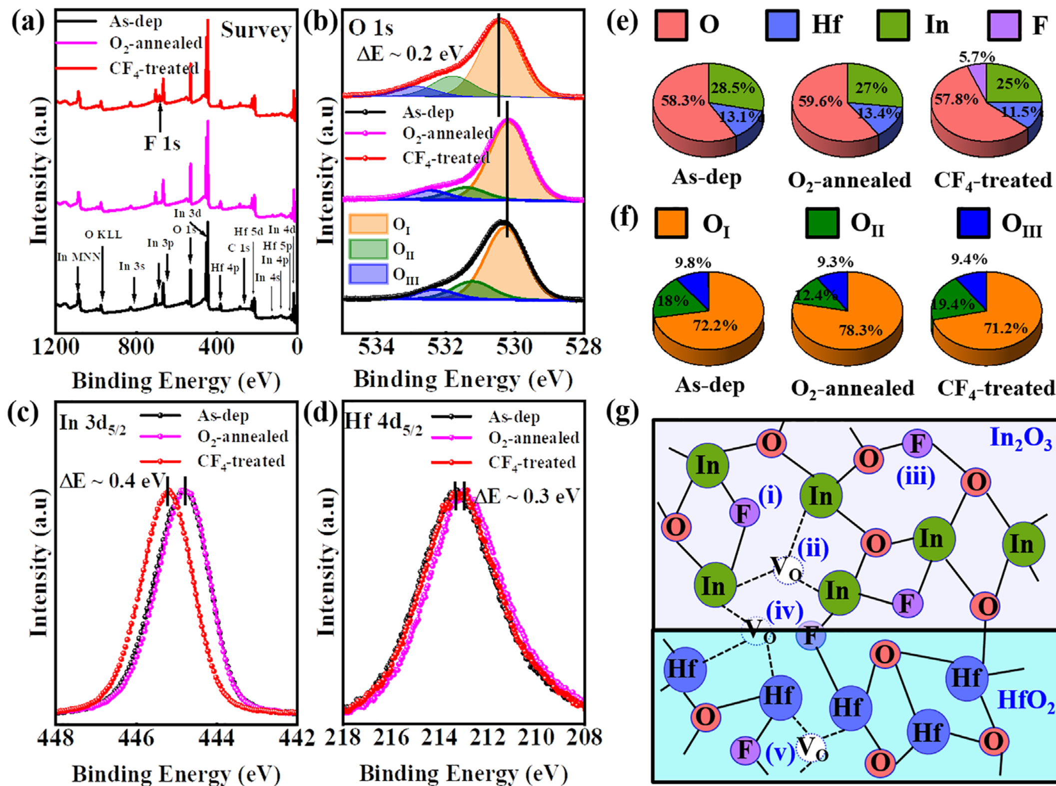

FIG. 5. XPS spectra of (a) survey, (b) O 1s, (c) In $3d_{5/2}$, and (d) Hf $4d_{5/2}$ core levels of the as-deposited, O_2-annealed (300 °C), and CF_4-treated (200 °C) In_2O_3/HfO_2 (1 nm/6 nm) heterostructures. (e) Composition analysis of In_2O_3/HfO_2 heterostructures. (f) Area percentage of deconvoluted sub-peaks from the O 1s spectra. (g) Schematic of F passivation mechanism: (i) F substituting O in bulk In_2O_3; (ii) F occupying O vacancy in bulk In_2O_3; (iii) excess F bonding with O in bulk In_2O_3; (iv) F passivating dangling bonds at In_2O_3/HfO_2 interface; (v) F passivating O vacancy in bulk HfO_2.

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samples. Composition analysis from the survey is summarized in Fig. 5(e), where oxygen content is increased in O_2-annealed samples, while CF_4-treated samples show a slight decrease in oxygen. Figure 5(b) shows the O 1s spectrum, which could be deconvoluted to three subpeaks: O_I (oxygen bound to metal), O_{II} (oxygen deficiency), and O_{III} (surface hydroxyl). It is interesting to note that the O 1s spectrum shifts to a higher binding energy (BE) by 0.2 eV accompanied by an increase in O_{II} area percentage [Fig. 5(f)] in CF_4-treated sample, while no shift and a decrease in O_{II} area percentage can be observed in O_2-annealed samples. This could be explained by more oxygen introduced via O_2 annealing, thereby increasing the oxygen content and decreasing the O_{II} area percentage.[25] On the other hand, CF_4 plasma could introduce F atoms into the heterojunction, and these F atoms could substitute the weakly bound oxygen, thus leading to a slightly decreased oxygen content and an increased O_{II} peak ratio and chemical shift.[15,18] This could also explain the positive shift of ∼0.4 eV observed in the In $3d_{5/2}$ spectrum [Fig. 5(c)] for CF_4-treated samples, suggesting a different chemical environment and the possible formation of In–F bonds.[26] The bond energies of In–F (506 kJ/mol) are much higher than that of In–O bond (346 kJ/mol),[18] possibly explaining the high gate bias stability in CF_4-treated TFTs.[16] Additionally, a negative shift of ∼0.3 eV can be observed in the Hf $4d_{5/2}$ spectrum [Fig. 5(d)] after 300 °C O_2 annealing, which could be an indicator for HfO_2 crystallization, explaining the high I_G in O_2-annealed TFTs. Fluorine has a similar ionic radius and stronger electronegativity than oxygen,[15,18] allowing for easy incorporation in oxides with minor distortion to the structure. It has also been reported that fluorine can substitute for an oxygen atom generating a free electron or passivate an oxygen vacancy site consuming a free electron.[15,16,18,26] The excessive fluorine may also form O–F bonds, acting as acceptor traps.[19] Based on this information, a passivation mechanism is proposed in Fig. 5(g), where the oxygen deficiencies and/or weakly bonded oxygen in the bulk In_2O_3 [processes (i), (ii), and (iii)], at the HfO_2/In_2O_3 interface [process (iv)], and/or in the bulk HfO_2 [process (v)] can be passivated by fluorine atoms.

In summary, we report the performance improvement of In_2O_3 TFTs via low-temperature CF_4/N_2O plasma treatment. It is found that the fluorination is more effective in reducing excessive electrons in In_2O_3 than oxidization, which can be explained by the fluorine passivating the oxygen vacancies. This study suggests that anion doping such as fluorine incorporation could be an effective method to improve the electrical performance of oxide semiconductor TFTs with ultrathin channel and dielectric. The work was supported by SRC nCore IMPACT Center, SRC/DARPA JUMP ASCENT Center, and AFOSR.

See the supplementary material for a comparison of fluorine passivation from literatures with our work and a comparison of the electrical performance of our fluorinated In_2O_3 TFTs with that of recently reported metal-oxide TFTs.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jie Zhang: Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Writing – original draft (equal). **Adam R. Charnas:** Formal analysis (equal); Validation (equal); Writing – original draft (equal). **Zehao Lin:** Formal analysis (equal); Validation (equal). **Dongqi Zheng:** Formal analysis (equal); Validation (equal). **Zhuozheng Zhang:** Data curation (equal); Formal analysis (equal); Validation (equal). **Pai-Ying Liao:** Data curation (equal); Validation (equal). **Dmitry Y. Zemlyanov:** Data curation (equal); Formal analysis (equal); Validation (equal). **Peide D. Ye:** Conceptualization (equal); Project administration (equal); Validation (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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